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10/762,864	01/21/2004	Wilson Wong	174/295	5928

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EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/762,864	WONG ET AL.	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/24/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1 - 32 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 7, 12 – 17, 26 and 28 - 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Gorecki (US 20040071205).

Re claims 1 and 26, Gorecki teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract) comprising: equalization implementation circuitry including a selectable number of taps, wherein the equalization implementation circuitry operates on the received data signal (Paragraph 0042, 0043);

programmable circuitry for allowing a first number of taps to be specified (Paragraph 0046); processing circuitry for computing a second number of taps (Paragraph 0044 – 0045); and selection circuitry for selecting one of the first and second numbers as the selectable number, wherein the selection circuitry is programmed to select only once while the equalization implementation circuitry operates on the received data signal (Paragraphs 0112 – 0117).

Re claim 2, Gorecki teaches of the selection circuitry being programmable to make its selection (Paragraph 0112).

Re claim 3, Gorecki teaches of the processing circuitry performing an algorithm to compute the second number (Paragraph 0045).

Re claim 4, Gorecki teaches of a memory coupled to the processor programmable logic device circuitry coupled to the processor circuitry and the memory (Paragraph 0112).

Re claims 5 - 6, Gorecki teaches of a printed circuit board comprising: a memory mounted on the printed circuit board and coupled to the programmable logic device circuitry (Paragraph 0112).

Re claim 7, Gorecki teaches of the printed circuit board further comprising: processor circuitry mounted on the printed circuit board and coupled to the programmable logic device circuitry (Paragraph 0112).

Re claims 12 and 28, Gorecki teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract) comprising: equalization implementation circuitry including at least one selectable coefficient value (Abstract); first processing circuitry for computing the coefficient value using a selectable starting value (after initialization, Paragraphs 0044 – 0045 and 0050), wherein the coefficient value is different from the starting value (after or during initialization, Paragraph 0050 - 0051); programmable circuitry for allowing a first starting value to be specified (initialization, Paragraph 0046 – 0047); second processing circuitry for computing a second starting value (initialization, Paragraphs 0044 – 0045 and 0050); and selection circuitry for selecting one of the first and second starting values as the selectable starting value, wherein the selection circuitry is controlled by a programmable element (Paragraphs 0112 – 0117).

Re claim 13, Gorecki teaches of the selection circuitry being programmable to make its selection (Paragraphs 0112 - 0113).

Re claim 14, Gorecki teaches of the first processing circuitry performing an algorithm to compute the coefficient value (Paragraphs 0044 - 0045).

Re claim 15, Gorecki teaches of the second processing circuitry performing an algorithm to compute the second starting value (Paragraphs 0044 - 0045).

Re claim 16, Gorecki teaches of a further programmable circuitry for allowing selection between (1) operation of the first processing circuitry to fix (*adjust*) on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt (*control or vary*) the coefficient value even after satisfactory equalization has been produced (paragraphs 0047, 0058, 0062 – 0065 and 0070).

Re claims 17 and 29, Gorecki teaches of a programmable logic device circuitry for adaptively equalizing a received data signal comprising: equalization implementation circuitry including at least one selectable coefficient value; processing circuitry for computing the coefficient value (see claim 12); and programmable circuitry for allowing selection between (I) operation of the processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced (see claim 16).

Claims 22 – 23 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaynes et al (US US 2005/0047779).

Jaynes teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Paragraph 0008, Figure) comprising: processing circuitry for computing an error signal using a selectable training pattern (#70, #72, Figure), wherein the processing circuitry operates on the received data signal (Figure); programmable circuitry for allowing a first training pattern to be specified (external process, Figure); training pattern circuitry for providing a second training pattern (operator, Figure); and selection circuitry for selecting one of the first and second training patterns as the selectable training pattern (external process or operator, Figure, Paragraph 0023), wherein the selection circuitry is programmed to select only once while the processing circuitry operates on the received data signal (Paragraphs 0008, 0022 – 0023).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8 – 11 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki in view of Lu (US 6,275,836).

Re claims 8 – 10 and 27, Gorecki teaches of a programmable logic device circuitry for adaptively equalizing a received data signal comprising: equalization implementation circuitry for adjusting or controlling the spacing of the taps (Paragraph 0043), wherein the equalization implementation circuitry operates on the received data signal; programmable circuitry for adjusting or controlling the spacing of the taps (Paragraph 0046); processing circuitry for adjusting or controlling the spacing of the taps (Paragraph 0044 – 0045); and selection circuitry for selecting one of the tap spacing (Paragraph 0112), wherein the selection circuitry is controlled by a programmable element to select only once while the equalization implementation circuitry operates on the received data signal (Paragraph 0112 – 0116). However, Gorecki does not teach of a programmable circuitry and processing circuitry for allowing a first selection between integer spacing and fractional spacing to be specified.

Lu teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract, Fig.3) comprising: equalization implementation circuitry including taps (interpolation filter) having a selected one of integer spacing and fractional spacing relative to the symbol rate of the data signal (Abstract, Lines 1 – 13, Fig.3); processing circuitry (#74, Fig.3) for computing a (second) selection (#76a, #76b, Fig.3) between integer spacing and fractional spacing (Abstract, Lines 9 – 13, Fig.3 and Col 7, Lines 17 – 29).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided the option to the user to choose between a fixed or fractional spacing depending on the incoming sampling rate for a good equalizer performance.

Re claim 11, Gorecki and Lu teach of all the limitations of claim 8. Lu teaches of the fractional spacing is a selectable fraction of the symbol period (1/fs, sampling rate fs, Col 7, Lines 48 – 62), wherein the first selection can include a programmably specified first fraction, and wherein the second selection can include a processing-circuitry-computed second fraction (see claim rejection above).

Re claims 24 – 25 and 32, Gorecki and Lu teach of a programmable logic device circuitry for adaptively equalizing a received data signal as discussed above in claims 8 – 11, comprising: equalization implementation circuitry having at least one sampling point with a selectable location relative to a bit period of the received signal; programmable circuitry for allowing a first location of the sampling point to be specified; processing circuitry for computing a second location of the sampling point; and selection circuitry for selecting one of the first and second locations as the selectable location. The symbol period of the tap spacings is the inverse of the sampling frequency. Changing the spacing will change the location of the sampling points.

Claims 18 – 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hillery (US 6,178,201) in view of Wang et al (US 6,693,958).

Re claims 18 and 30, Hillery teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract) comprising: equalization implementation circuitry responsive to an error signal (Fig.1), wherein the equalization implementation circuitry operates on the received data signal (#22, Fig.1); first processing circuitry for computing a first decision directed error signal (#40, Fig.1, Col 3, Lines 54 – 67); second processing circuitry for computing a second error (#38, Fig.1, Col 3, Lines 38 – 50); and selection circuitry (#36, Fig.1) for selecting one of the first and second error signals as the error signal (Col 3, Lines 30 – 37), wherein the selection circuitry is programmed to select only once while the equalization implementation circuitry operates on the received data signal (Col 4, Lines 16 – 32, *the selection circuitry is programmed to select only once in steady conditions to compensate for distortions in the input signal*). However, Hillery teaches of the differences between blind and non-blind adaptive equalizers (Col 1, Lines 45 – 56) but does not specifically teach of the second processing circuitry computing the error by the use of a training pattern.

Wang teaches of an adaptive channel equalizer (#50, Fig.1) for processing a demodulated VSB signal containing terrestrial broadcast high definition television information operates adaptively in blind, training, and decision-directed modes (Abstract). When the equalizer operation is initiated, the coefficient values (filter tap

weights) are usually not set at values which produce adequate compensation of channel distortions. In order to force initial convergence of the equalizer coefficients, a known "training" signal may be used as the reference signal. Training signals, eg., a pseudorandom number (PN) sequence, have been used extensively in telecommunications devices such as television receivers and telephone modems. A major benefit of employing a known PN sequence training signal in the transmission is that errors can be accurately obtained, and the equalizer can be trained to equalize the transmission channel before and during transmitting and receiving data (Col 1, lines 60 – 67 to Col 2, Lines 1 – 10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a training sequence to compute the error for the benefit of more accurate measurements compared to computing the error without a training sequence.

Re claim 19, Hillery teaches of the selection circuitry being programmable (#34, Fig.1) to make its selection (Col 4, Lines 16 – 32).

Re claim 20, Hillery teaches of the first processing circuitry performs an algorithm (LMS) to compute the first decision directed error signal (Col 3, Lines 65 – 67).

Re claim 21, Hillery teaches of the second processing circuitry performing an algorithm (CMA) to compute the second error signal using a training pattern (Col 3, Lines 45 – 47).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 6:30 - 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER